
ECE 436 Laboratory 7

FINAL PROCESSOR DESIGN

Description:

Now that you have your cache and pipeline designs, you need to put everything together including final ISA modifications, dealing with hazards, stalls, and the memory hierarchy. Based on your processor design, perform the necessary revisions to your IPC analysis. I will expect a fully functioning processor that runs all the available benchmarks and has at a minimum: some change to the ISA, some level of pipelining, and some cache. Any other changes to the design are more than welcome (e.g. superscalar). The choices of ISA modifications, pipelining and cache design need to be justified by your quantitative analysis from the previous labs. Definitely do not choose to only make the minimum changes (e.g. add NOP to the ISA, two-level pipelining, direct-mapped I-cache only) and expect a good grade, a good grade will require more than minimum effort. An example good set of choices might be: add hardware multiplier, 5-level pipeline, and direct-mapped I- and D-caches with 32-bit blocks with burst-mode SDRAM controller. But the final result that matters will be given by your processor's performance: I will rank the projects based on the figure of merit $\text{Performance} = 1/(\text{CPI} * \text{Tclk})$, where CPI is the average CPI for all 15 benchmarks (simply compute the CPI for each benchmark, then take the average of that), and Tclk is the period of the maximum clock frequency at which your processor runs (if the processor runs at 50MHz then $\text{Tclk} = 20\text{ns}$ as we don't have a good method of testing at higher clock frequencies). I have decided to ignore the area penalty as long as your design fits, with the exception of cache size which should still be limited to 8 cache lines of between 2 to 8 bytes for unified or I-cache only, and 8 cache lines each for separate I- and D-caches.

The top 3 "speed demons" will get some bonus points.

Deliverables:

There are 3 deliverables for this lab:

- A presentation
- A demo
- A final report

Presentation:

- Should take about 15 minutes (i.e. <15 slides)
- Each team member should present some part
- Use Classroom Presenter
- Show your original Gantt chart and how close you followed it
- Explain each team members role in the project (1 slide for this and Gantt chart)
- Briefly present your original design (schematic vs. VHDL at top level, State-chart vs VHDL for controller, average CPI and Tclk, perceived bottlenecks) (1-2 slides)
- Briefly describe your design decisions and the quantitative arguments for those decisions (e.g. use the CPI and instruction frequencies in the various benchmarks) (1-2 slides)
- Present your final design (2-3 slides)
- Present an analysis of your final design which shows the improvements over original, including the average CPI and the minimum Tclk (1-2 slides)
- After the presentation also upload an electronic version on the class web site of your entire design, including presentation and journal

Demo:

- All 15 benchmarks running at the maximum clock frequency for your design.
- Demonstrate how you calculate your average CPI on 1-2 benchmarks chosen arbitrarily from the set.
- Report the average CPI for each benchmark and the minimum Tclk
- Each student upload a text file with names of all team members for the group a point score for each team member such that the total is 100 based on contribution to project